This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend claims 1, 2, 5 and 6 to read as follows. Claims 3 and 4 remain unchanged.

1. (Currently amended) A method of protecting an integrated circuit from over voltage, the method comprising:

accepting a voltage from a power supply input to the integrated circuit;

accepting a pad voltage from an external voltage source;

comparing the power supply voltage to a predetermined value;

coupling a bias voltage for the integrated circuit to a gate of a PMOS (P-channel Metal Oxide Semiconductor) device when the power supply is below the predetermined value; and

coupling the pad voltage to [~~the bias~~] a bias mid node to provide the bias voltage for the integrated circuit when the power supply is below the predetermined value.

2. (Currently amended) A method as in claim 1 wherein coupling the pad voltage to the bias mid node [~~the generation of the bias voltage~~] comprises:

coupling the pad voltage into a drain of [~~a~~] the PMOS [~~(P-channel Metal Oxide Semiconductor)~~] device[~~; and~~

~~coupling the power supply voltage into a gate of the PMOS device~~].

3. (Currently Amended) A method as in claim 2 wherein [~~using the pad voltage to generate a~~] coupling the pad voltage to the

bias_mid node to provide the bias voltage for the integrated circuit further comprises using the source voltage of the PMOS device to couple the pad voltage to the [~~bias voltage~~] bias_mid node.

4. (Previously amended) A method as in claim 2 wherein coupling the pad voltage into the drain of a PMOS (P-channel Metal Oxide Semiconductor) device comprises:

providing the pad voltage to an input of a plurality of diode connected MOS devices; and

coupling an output of the plurality of diode connected MOS devices to the drain of the PMOS device.

5. (Currently amended) A method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present the method comprising:

providing V_{DDO} to a control electrode of a first semiconductor device;

providing bias_mid to an input electrode of the first semiconductor device such that the first semiconductor device will turn off when V_{DDO} - bias_mid [~~V_{DDO} exceeds~~] is less than the threshold of the first semiconductor device; and

actuating a switch in response to the turn off of the first semiconductor device to couple Vpad to bias_mid.

6. (Currently amended) The method of claim 5 wherein actuating a switch in response to the turn off of the first semiconductor device to couple Vpad to bias_mid [~~using the turn off of the first semiconductor device to couple Vpad to bias_mid further~~] comprises:

turning on a second semiconductor device and turning off a third semiconductor device which are coupled together thereby providing a turn on voltage for a fourth semiconductor device; and

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using the turn on of the fourth semiconductor device to couple Vpad to bias_mid.